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Droop Compensation with Soft Switching for High Voltage Converter Modulator (HVCM)

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***Abstract*—High Voltage Converter Modulators (HVCM) offer significant performance advantages over conventional modulator technologies for long pulse applications. One of the key advantages of HVCM technology is the ability to compensate for capacitor bank voltage droop. Achieving droop compensation without incurring significant additional switching loss has not been possible in existing designs. This paper presents an analysis of the "Y-point" variant of the HVCM topology using the Combined Phase and Frequency Modulation (CPFM) technique. This, combined with the addition of a 'lossless' snubber circuit, enables droop compensation while achieving soft switching over the entire pulse duration. The rise time and overshoot of the output voltage pulse is optimised using an iterative extreme seeking algorithm. The optimisation reduces the rise time from 100μs to 50μs with no overshoot. This will lead to an increase in overall accelerator efficiency.**

I. Introduction

The first generation of HVCMs were developed at the Los Alamos National Laboratory for the Spallation Neutron Source (SNS) at Oak Ridge. One of the problems encountered during development was that the Y-point of the high voltage transformer was subject to large voltage spikes, caused by switching transients, which would eventually result in transformer insulation failure. The chosen solution to this problem was to connect the Y point to the center point of the DC-link shown in Figure 1. However, this connection changes the operation of the resonant circuit [1] so that the circuit is operating in resonant mode for less than 40% of the cycle. In this paper, the application of CPFM is analysed with the quasi-resonant operation of the 'Y point' variant. An extremum seeking-based optimisation technique is used to "tune" the switching edges in order to achieve very fast rise time without overshoot. Results are presented showing that a flat output pulse can be produced even in the presence of significant DC-link voltage droop.

II. Modulation Schemes for Droop Compensation

There are several different modulation techniques that can be used to control the output voltage of the HVCM for droop compensation, pulse shaping etc. as shown in [2].

A. 'dead time' modulation proposed for SNS prototype

For the first generation of HVCMs, the modulation scheme achieved output voltage control by varying the 'dead time' period (all IGBTs OFF) of a fixed frequency waveform. One problem with this fixed frequency scheme is that it is impossible to maintain soft switching over the full range of operation. Another undesirable feature of the dead time scheme is that the H-Bridge output voltage is defined by the load during the dead time period and as a result energy can flow back into the DC-link, resulting in higher conduction losses. For this reason the 'dead time' PWM droop compensation was abandoned [1].

B. Combined Phase and Frequency Modulation

The Combined Phase and Frequency Modulation (CPFM) technique proposed in [2] achieves soft switching for all transitions over the duration of the pulse. However, the implementation of CPFM described in [2] cannot be directly applied to the first generation (Y-point) HVCMs because of the different modes of operation [1] for the two implementations. The circuit analysis for the 'Y-point' HVCM variant is very different from that of the fully resonant topology presented in [2]. It can be shown that with the application of the CPFM method, soft switching can be achieved for all switching transitions and over the full operational range.

III. Circuit Analysis

The circuit analysis presented in [2] is not valid for the Y-Point connected (SNS, KAERI) variant, a different approach must be used. The circuit used for analysis is shown in Figure 1. The voltage sources E_a, E_b & E_c represent the H-bridge output voltages referred to the secondary of the HV transformers. The capacitances C_a, C_b & C_c represent the lumped capacitance which is a combination of the "resonant peaking capacitor", C_{rp} and the rectifier parallel capacitors.

During the resonant part of the circuit operation both of the HV diodes are OFF. So the effective capacitance, $C_a, C_b, C_c = C_p$ across each secondary winding during the resonant mode is $C_p = C_{rp} + 2C_{\text{rect}}$. Figure 2 shows the equivalent circuit used for the analysis. The inductances L_a, L_b & L_c represent the transformer leakage inductance referred to the secondary.

The assumptions for the analysis are as follows.

1) The current in (output filter choke) is virtually smooth, hence it can be replaced by a current sink for analysis of value I_o (where I_o is the load current).

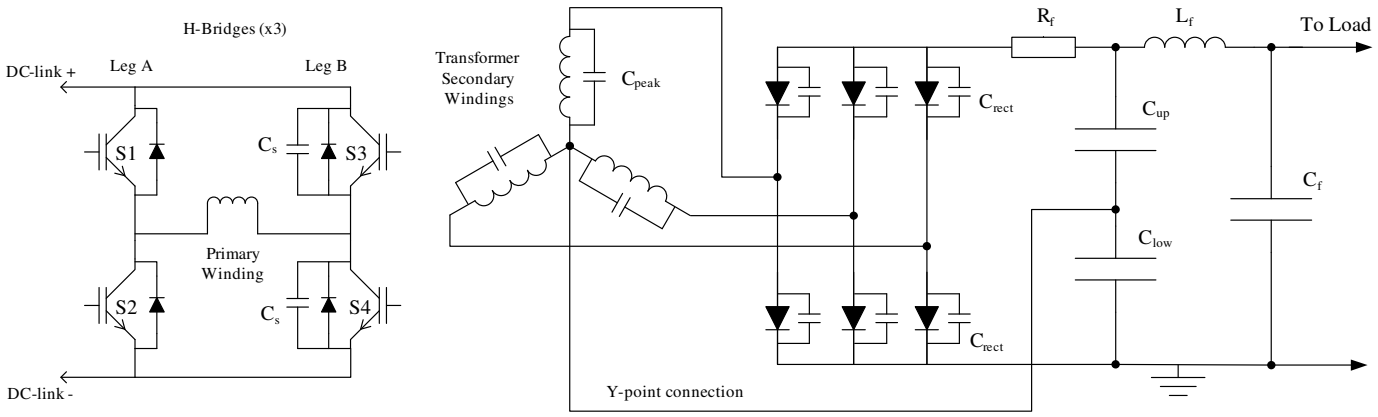

Fig. 1. Schematic of HVCM

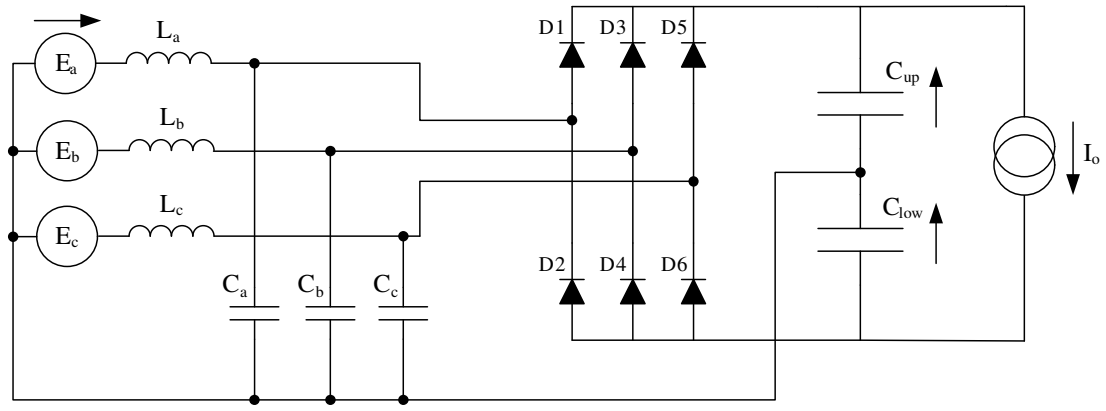

Fig. 2. Equivalent circuit for analysis (the analysis is performed assuming a positive output voltage)

2) The voltages across $C_{\rm up}$ and C_{low} (output filter capacitors) are constant and equal. This value is denoted as V, such that the converter output is $2V$.
3) Diodes are ideal with no voltage drop or capacitance. (These effects can be included later if required).
4) Transformer resistance and core loss are neglected.
5) The IGBTs switch instantaneously and the soft switching capacitors are omitted.

The analysis proceeds by identifying the modes of circuit operation, corresponding to the various different diode conduction patterns as in [1]. However the modes are different from the ones described in [1] due to the CPFM. Figure 3 shows simulated waveforms with the different modes of operation.

Mode 1: This mode starts when the H-bridge switches from 0 to +E. To achieve soft switching this transition must coincide with the zero crossing of I_a. As D1 and D2 are both OFF during Mode 1 La & Ca are free to resonate. V_a undergoes a resonant reversal from $-E$ toward $2E+V$. However, when it reaches $+V$, diode D1 becomes forward biased and turns ON changing the circuit topology. This ends Mode 1. The voltage V_a during Mode 1 is given by

$$V_a = E - (E+V)\cos(\omega_0 t), \qquad \omega_0 = \frac{1}{\sqrt{LC_p}} \tag{1}$$

The duration for Mode 1 is given by the solution to

$$\omega_0 T_1 = \arccos\left(\frac{E-V}{E+V}\right) \tag{2}$$

For the circuit parameters and conditions considered, $(E+V) \gg (E-V)$ and Mode 1 always lasts for just more than $\frac{1}{4}$ of a resonant cycle. To avoid carrying through the inverse trigonometric function, it is justifiable to assume that Mode 1 lasts for exactly $\frac{1}{4}$ of a resonant cycle. T_1 is then given by

$$T_1 = \frac{\pi}{2}\sqrt{LC_p} \tag{3}$$

The peak current drawn from the H-bridge $(\hat{I})$ occurs at the end of Mode 1 and can be calculated to be

$$\hat{I} = (E+V)\sqrt{\frac{C_p}{L}} \tag{4}$$

This represents the peak IGBT current reflected by the transformer turns ratio.

Mode 2: This starts when V_a reaches V and D1 turns ON. During Mode 2 the voltage across L_a is $(E_a - V = E - V)$ this causes the current I_a to decrease linearly. Mode 2 ends when E_a changes from $+V$ to 0. The time T_2 is given by equation (5)

$$T_2 = \frac{T_s}{2} - T_1 - T_3 \tag{5}$$

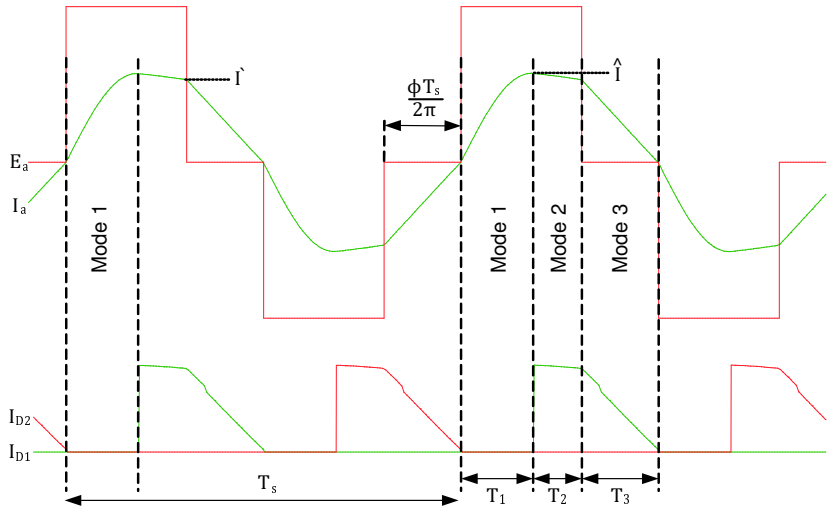

Fig. 3. Simulated waveforms showing modes of operation

$$T_2 = \frac{T_s}{2} - \frac{\pi}{2}\sqrt{LC_p} - \frac{\phi T_s}{2\pi} \tag{6}$$

I' is the current at the end of Mode 2, I' is given by

$$I' = \hat{I} - \frac{(V-E)T_2}{L} \tag{7}$$

Mode 3: This starts when E_a changes from $+V$ to 0. The voltage across L_a is $(E_a - V = -V)$ during Mode 3 so I_a decreases linearly to zero. The duration of Mode 3 is defined as

$$T_3 = \frac{\phi T_s}{2\pi} \tag{8}$$

To achieve soft switching the volt-second product across L_a for half the switching period (T_S) must equal zero.

$$\int_0^{T_1}(E - V_a)\mathrm{d}t + (E-V)T_2 - VT_3 = 0 \tag{9}$$

By substituting equations (1) - (8) into (9) and solving the integral the condition for Zero Current Switching (ZCS) of the lagging leg of the H-bridge can be rewritten

$$f_s = \frac{\frac{\phi E}{\pi} - E + V}{[E(2-\pi) + V(2+\pi)]\sqrt{LC_p}} \tag{10}$$

Meeting this condition sets the relationship between the switching frequency (f_s) and the phase shift between the two legs of the H-bridge (ϕ).

A. Phase and Frequency Relationship

We can equate $P_{in} = P_{out}$ (assuming negligible losses). In steady state the power supplied by one phase is equal to $\frac{1}{3}$ of the power supplied to the load.

$$\frac{P_{\text{out}}}{3} = \frac{2}{T_s}\left[\int_0^{\frac{\pi}{2\omega_0}} E\hat{I}\sin(\omega_0 t)\mathrm{d}t + T_2 E\left(\frac{\hat{I}+I'}{2}\right)\right] \tag{11}$$

By combining equations (1) - (11) and substituting $V = \frac{V_{out}}{2}$ & $E = NV_{\text{dc}}$, after some manipulation yields

$$\phi = \frac{a_4E^4 + a_3E^3 + a_2E^2 + a_1E + \sqrt{b_4E^4 + b_3E^3 + b_2E^2 + b_1E}}{c_4E^4 + c_3E^3 + c_2E^2 + c_1E} \tag{12}$$

where $E = NV_{\text{dc}}$ and the 12 constants a_{1-4}, b_{1-4} & c_{1-4} are defined in terms of the circuit parameters V_{out}, R_{load}, N, L & C_p.

IV. Upgrades to HVCM Prototype

Soft switching capacitors were added to an existing HVCM prototype as shown on Leg B in Figure 1. Further analysis for the determination of the required capacitor value is presented in [3]. As the prototype was not designed to work with CPFM the power circuit is suboptimal, but time and budget constraints did not allow for a complete rebuild. The unconventional layout of the H-bridge 'switch plate' assembly made it impossible to mount the soft switching capacitors directly on the IGBT modules for minimum inductance. Instead, the soft switching capacitors are mounted above the gate drive boards and connected to the IGBTs using flat busbars in order to prove the above presented concept. In addition to the power circuit changes a new controller, based on the Texas Instruments TMS320F28335, has been added to produce the PWM for CPFM.

A. Rise Time Optimisation Using Extremum Seeking

Fast rise time leads to improved accelerator efficiency and increases the available power to the beam. Existing controller designs have relied on manual tuning of the start pulses to avoid overshoot. Using this 'staggered start' method the rise time was limited to around $100\mu s$. An extremum seeking-based optimisation algorithm [4] was used to 'tune' the first eight switching edges on each phase (24 parameters total) to achieve a rise time of $50\mu s$ with no overshoot. This method can also be employed to produce any pulse shape (within

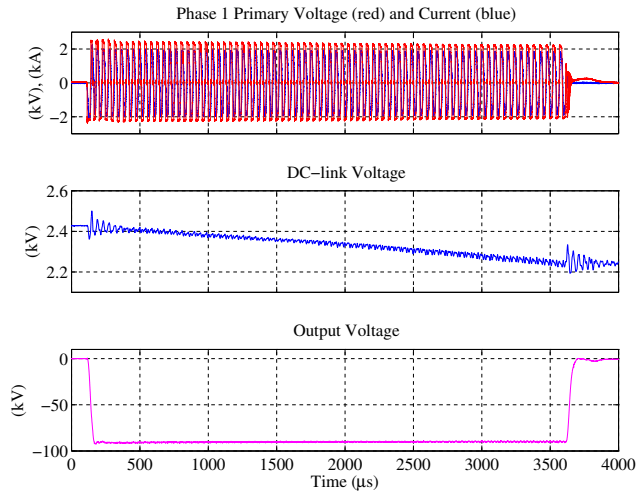

Fig. 4. Waveforms from SNS prototype modulator showing 3.5ms flat-top output pulse while the DC-link droops by around 8%

Pulse Voltage	90kV
Pulse Current	73A
Pulse Length	3.5ms
Rise Time	50μs
Load Impedance	1236Ω
DC-link Voltage	2428V
DC-link Voltage droop	8%
Flat Top	1%
Ripple	1%

TABLE I
CONDITIONS AND PARAMETERS FOR PULSE SHOWN IN FIGURE 4

physical limitations). Details of the optimisation will be given in [5].

V. RESULTS

Figure 4 shows waveforms from the adapted HVCM prototype during a 3.5ms pulse. Looking at Figure 4 it can be seen that the pulse flat top is maintained while the DC-link voltage droops by 8%. The waveforms in Figure 5 show the soft switching of the IGBTs at the start and the end of the pulse.

VI. NEXT GENERATION HVCM

Since their installation many improvements have been made to improve the reliability of the HVCMs at SNS [6]. However, modulator technology would greatly benefit from a new generation of HVCMs designed using modern techniques and components. The new generation of HVCMs will benefit from the lessons learned at SNS and KAERI and inherently include new techniques such as CPFM, Planar DC-link bus and modular HV transformers. The new modular designs will be simpler to manufacture which will reduce the capital cost of HVCMs. The new techniques based on analytical analysis and parameter optimisations simplify and speed up the design process [7]. These significant changes in design are required to bring HVCM technology to the level of maturity that is

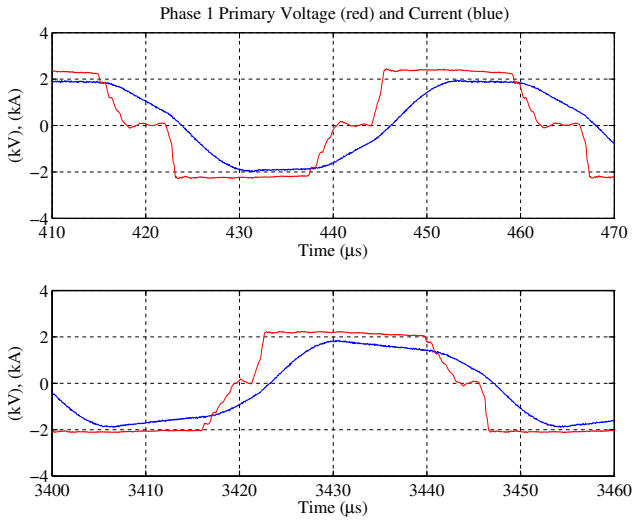

Fig. 5. Waveforms showing IGBT soft switching at start and end of pulse

required to fully exploit the potential benefits for accelerator facilities.

VII. CONCLUSION

The differences between the fully resonant HVCM and the 'Y Point' variant have been outlined. An analysis of the 'Y point' HVCM operating with CPFM soft switching has been shown. Results from an adapted HVCM prototype show that CPFM can compensate for significant DC-link capacitor droop while maintaining a flat output pulse. Outlines of improvements to HVCM design for the next generation have been given. The inherent advantages and ongoing research into HVCM technology is rapidly bringing it to a level of maturity that makes it the logical choice for many long pulse applications.

REFERENCES

[1] W. A. Reass, D. M. Baca, R. F. Gribble, D. E. Anderson, J. S. Przybyla, R. Richardson, J. C. Clare, M. J. Bland, and P. W. Wheeler, "High-frequency multimegawatt polyphase resonant power conditioning," in *IEEE Transactions on Plasma Science*, Aug 2005.

[2] M. J. Bland, J. C. Clare, P. Zanchetta, P. W. Wheeler, and J. S. Pryzbyla, "A high frequency resonant power converter for high power RF applications," in *11th European Conference on Power Electronics and Applications*, 2005.

[3] F. Carastro, J. C. Clare, M. J. Bland, and P. W. Wheeler, "Calorimetric loss measurements and optimization of high power resonant converters for pulsed applications," in *13th European Conference on Power Electronics and Applications*, 2009.

[4] A. Scheinker and M. Krstic, "A universal extremum seeking-based stabilizer for unknown LTV systems with unknown control directions," in *Proc. ACC*, Montreal, Canada, 2012.

[5] A. Scheinker, M. Bland, M. Krstic, and J. Audia, "Extremum seeking-based optimization of high voltage converter modulator rise-time," in *Publication Pending*, 2012.

[6] D. E. Anderson, J. Hicks, D. Hurst, E. Tapp, M. Wezensky, D. Baca, and W. Reass, "Enhancements for the 1MW high voltage converter modulator systems at the sns," in *Particle Accelerator Conference*, Knoxsville, TN, 2005.

[7] J. Chao, M. Bland, A. Watson, P. Zanchetta, J. Clare, P. Wheeler, and W. Reass, "Optimisation and comparison of two soft switched high voltage converter modulator topologies," in *Publication Pending*, 2013.